

Amendments to the Drawings:

Figs. 7 and 9 have been amended to include the "Prior Art" label. Substitute sheets including the amended Figs. 7 and 9 are included herewith. Additionally, red-lined sheets, showing the amendments made to Figs. 7 and 9, are additionally included herewith.

Attachment: Two (2) Replacement Sheets

Two (2) Annotated Sheets Showing Changes

Remarks:

Applicants appreciatively acknowledge the Examiner's confirmation of receipt of Applicants' claim for priority and certified priority document under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application is respectfully requested.

Claims 1 - 12 are presently pending in the application.

Claims 4 - 6 and 11 - 12 are subject to examination and claims 1 - 3 and 7 - 10 have been withdrawn from examination. Claims 2, 4 - 6, 7, 9 and 11 - 12 have been amended.

Applicants gratefully acknowledge that claims 11 - 12 have been indicated as being allowed. Claims 11 - 12 have been amended to recite a MOS transistor, rather than a PMOS transistor. It is believed that the present amendment should not effect the allowability of these claims.

In item 4 of the above-identified Office Action, the drawings were objected to for not including the legend "Prior Art" in connection with Figs. 7 and 9. Figs. 7 and 9 have been amended to include the "Prior Art" label. Substitute sheets including the amended Figs. 7 and 9 are included herewith. Additionally, red-lined sheets, showing the amendments made to Figs. 7 and 9, are additionally included herewith.

In item 5 of the Office Action, Applicants' cooperation was requested in correcting any errors of which Applicants become aware in the specification. Applicants note that the specification has been amended herein to make reference to an NMOS transistor, rather than a PMOS transistor. It is believed that no new matter is added by way of these amendments for the following reason. It is known in the art that a PMOS-transistor is defined as a MOS-transistor having a p-conducting source and drain regions in an n-conducting well, and that an NMOS-transistor is defined as a MOS-transistor having n-conducting source and drain regions in a p-conducting well. This definition can be seen for example, from Fig. 1 of DE 195 26 183 C1, which is cited on page 1, line 25 of the instant application. In reviewing the instant application, it is clear that Fig. 1 of the instant application shows a MOS-transistor having a source region 13 which is n^+ -doped (See Fig. 1B and page 14 of the instant application) and a p-conducting well 12 (12a, 12b). In other words, in accordance with the above-definition, the MOS-transistor described in the present application, and shown in the drawings, **is actually an NMOS-transistor**, and not a PMOS transistor, as it was originally labeled. Applicants have amended the specification papers to reflect the above facts, as well as to correct other, minor errors. In light of the foregoing, and in view of the drawings and terminology in the art, it can be seen that no new matter is added by way of these amendments.

In item 7 of the Office Action, claims 4 - 6 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U. S. Patent No. 6,794,251 to Blanchard ("BLANCHARD").

Applicants respectfully traverse the above rejections.

More particularly, Applicants' have amended claim 4 to more particularly point out the invention of that claim.

Applicants' amended claim 4 now recites:

In a MOS field-effect transistor cell having an epitaxial layer in which a gate region and a source region are formed below a polysilicon layer, said gate and source regions defining a channel zone in said epitaxial layer below the polysilicon layer, wherein a body zone in the source region extends deeper into the epitaxial layer than that in the gate region and an impurity concentration of the body zone in the source region is greater than an impurity concentration of the body zone in the gate region, the improvement which comprises:

the polysilicon layer having holes formed in the gate region and pillars formed in the source region.
[emphasis added by Applicants]

As such, Applicants' claim 4 requires, among other limitations, a polysilicon layer that is provided on top of an epitaxial layer, including a gate region and a source region forming a channel zone. The body region of the source region of the claimed device extends deeper into the epitaxial layer than the body region of the gate region, and an impurity

concentration of the body region of the source is greater than the impurity concentration of the body region of the gate.

In this device set forth in the preamble of claim 4, and incorporated into the body of claim 4 by reference to the polysilicon layer, gate region and source region, claim 4 further requires the polysilicon layer to have holes formed within the gate region and pillars in the source region.

Applicants respectfully disagree that the above claimed invention is taught or suggested in the **BLANCHARD** reference.

More particularly, **BLANCHARD** fails to teach or suggest, in the semiconductor device claimed by Applicants, a polysilicon layer to have holes formed within the gate region and pillars in the source region. Rather, **BLANCHARD** discloses an NMOS (not a PMOS) field effect transistor including a body zone of a source region that extends deeper into an epitaxial layer than the body zone of a gate region, the impurity concentration of the body zone of the source region being greater than that of the impurity concentration of the body zone of the gate region. In the Office Action, an insulated gate electrode of the NMOS field effect transistor, formed as a polysilicon gate, is alleged to be Applicants' claimed polysilicon layer on top of the channel zone layer.

Applicants respectfully disagree.

BLANCHARD neither teaches, nor suggests that the polysilicon gate of BLANCHARD includes holes in a gate region and pillars in a source region, as required by Applicants' claim 4.

Further, the pillars 40, pointed to in the Office Action, are not in the alleged polysilicon region, (i.e. the polysilicon gate 18 of BLANCHARD).

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 4 and 11. Claims 4 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 4 or 11.

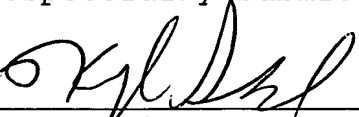
In view of the foregoing, reconsideration and allowance of claims 4 - 6 and 11 - 12 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to
Sections 1.16 and 1.17 to the Deposit Account of Lerner and
Greenberg, P.A., No. 12-1099.

Respectfully submitted,



For Applicants

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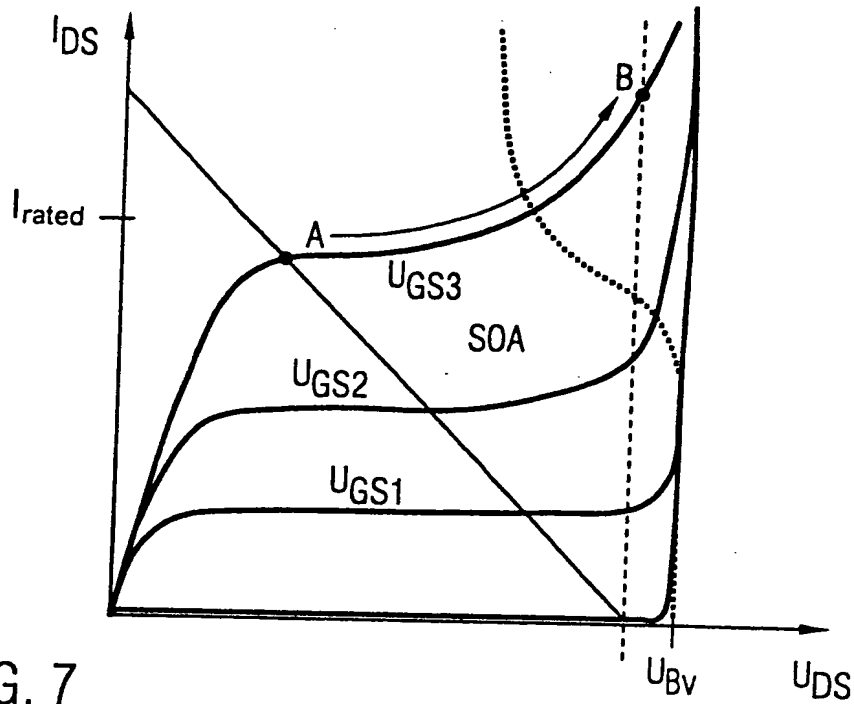


FIG. 7
 PRIOR ART

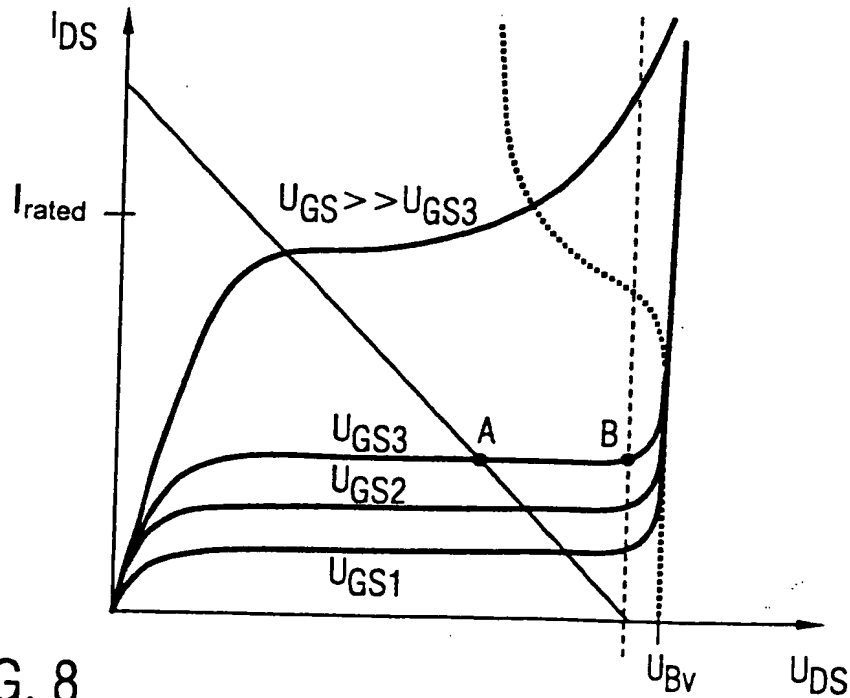


FIG. 8

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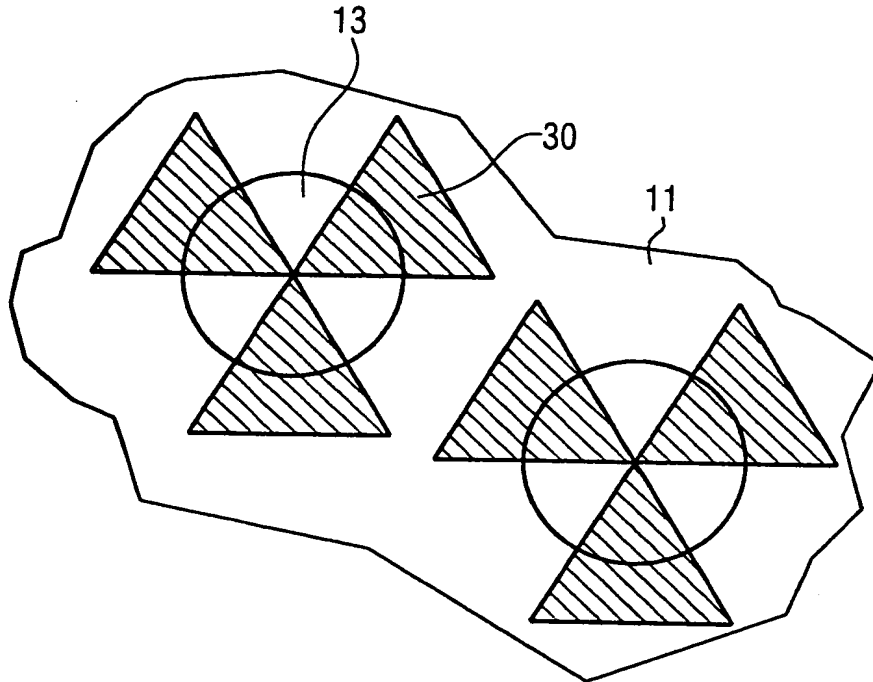


FIG. 9
PRIOR ART